ABSTRACT OF THE DISCLOSURE

A semiconductor memory device according to the present invention includes isolations, active regions, control gate electrodes and floating gate electrodes. The isolations are formed on a semiconductor substrate. The active regions are defined on the semiconductor substrate and isolated from each other by the isolations. The control gate electrodes are formed over the semiconductor substrate. Each of the control gate electrodes crosses all of the isolations and all of the active regions with a first insulating film interposed between the control gate electrode and the semiconductor substrate. Each of the floating gate electrodes is formed for associated one of the active regions so as to cover a side face of associated one of the control gate electrodes with a second insulating film interposed between the floating gate electrode and the control gate electrodes. In this device, the isolations are spaced apart from each other along the width of the control gate electrodes and each of the isolations crosses all of the control gate electrodes and extends continuously along the length of the control gate electrodes.